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EXAMINER	
TO, TUYEN P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 05/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

ND

Office Action Summary	Application No.	Applicant(s)	
	10/648,231	TANAKA ET AL.	
	Examiner	Art Unit	
	Tuyen To	2825	TT

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _03_ MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _18 April 2006_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-16_ is/are pending in the application.

4a) Of the above claim(s) _17-18_ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _1-16_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _27 April 2003_ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This is a response to the communication filed on 4/18/2004.

1. **Claims 17-18** have been withdrawn.

2. **Claims 1-18** are pending.

3. Applicants' election of **Group I (claims 1-16)** in the reply filed on 04/18/2006 is acknowledged. Because applicants did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Specification

4. The disclosure is objected to because of the following informalities:

On page 36 (lines 6-7), "Fig. 5A" appears to be a typographical error. It should be Fig. 15A.

On page 7 (line 5) "anormality" appears to be a typographical error.

On page 17 (line 5) "electron bean" appears to be a typographical error

Appropriate correction is required.

Drawings

5. The drawings are objected to because in Fig. 18, the "ANORMALITY" inside element 502 appears to be a typographical error.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure

number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 1-6 and 9-14** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al. ("Shishido") (Pub. No. 2003/0015660) in view of Ponnapalli et al. ("Ponnapalli") (US Patent No. 6,175,947).

Claim 1 and similarly recited claim 9, Shishido discloses a system and a method (claim 9) for evaluating a semiconductor device pattern, comprising:

feature index calculating means for quantifying a property of a three-dimensional shape of each pattern to be evaluated, as feature index (Figs. 1 and 14; abstract; paragraphs [0028]-[0029]);

However, Shishido does not discloses:

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index ; and

device property estimating means for estimating properties of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by said feature index calculating means, and the information recorded in the database stored in said database storing means.

Ponnapalli discloses:

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index (Fig. 2; col. 3, line 23 to col. 4, line 20 ; col. 5, line 55 to col. 6, line 32); and

device property estimating means for estimating properties ("capacitance") of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape, which have been quantified by said feature index calculating means, and the information recorded in the database stored in said

database storing means (Fig. 2;col. 3, line 23 to col. 4, line 20; col. 5, line 55- col. 6, line 32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Shishido with Ponnapalli because the combined teaching which including a database contains a library of pre-computed parasitic values (electrical properties) for each 3-D pattern of wiring and extracting (estimating) the capacitance and inductance (electrical properties) of patterns based on their corresponding pattern indices and the stored information (Fig. 2;col. 3, line 23 to col. 4, line 20; col. 5, line 55- col. 6, line 32) would provide an accurate and speedy computation of interconnect parasitic values both before and after performing a detailed wiring of an IC chip (col. 3, ll. 6-11) .

Referring to claim 2, Shishido discloses a system for evaluating a semiconductor device pattern, comprising:

feature index calculating means including,

electron beam irradiating means for irradiating a converged electron beam onto a pattern to be evaluated, while scanning the same (Fig. 10, paragraphs [0097]-[0099]);

secondary electron detecting means for detecting secondary electrons produced from the pattern by the irradiation of the electron beam by said electron beam irradiating means (Fig. 10, paragraphs [0097]-[0099]); and

signal arithmetic processing means for dividing a signal waveform of the secondary electrons detected by said secondary electron detecting means into a plurality of regions, based on an amount of change in signal amount, and quantifying a

property of a three-dimensional shape of the pattern to be evaluated, as a feature index on the basis of the size of said each divided region (figs. 11 and 25, paragraphs [0099]-[0100]) ;

However, Shishido does not discloses:

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index; and

device property estimating means for estimating a property of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape quantified by said feature index calculating means, and the information recorded in the database.

Ponnapalli discloses:

database storing means for storing a database that records therein a relationship between feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index (Fig. 2; col. 3, lines 23 to col. 4, line 20 ; col. 5, line 55- col. 6, line 32); and

device property estimating means for estimating a property of a device circuit formed by the pattern to be evaluated, on the basis of the feature indices of the three-dimensional pattern shape quantified by said feature index calculating means, and the information recorded in the database (Fig. 2;col. 3, line 23 to col. 4, line 20; col. 5, line 55- col. 6, line 32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Shishido with Ponnapalli because the combined teaching which including a database contains a library of pre-computed parasitic values (electrical properties) for each 3-D pattern of wiring and extracting (estimating) the capacitance and inductance (electrical properties) of patterns based on their corresponding pattern indices and the stored information (Fig. 2;col. 3, line 23 to col. 4, line 20; col. 5, line 55- col. 6, line 32) would provide an accurate and speedy computation of interconnect parasitic values both before and after performing a detailed wiring of an IC chip (col. 3, ll. 6-11) .

Referring to claim 3, the system according to claim 2, wherein said secondary electron detecting means detects a plurality of secondary electrons different in angle formed by the electron beam irradiated from said electron beam irradiating means and the surface of the pattern to be evaluated (Shishido, Fig. 10, par. [0098], the tested wafer is continuously moved in X and Y directions, i.e. detecting electron beam from different angles).

Referring to claim 4, the system according to claim 2, further including back scattered electron detecting means for detecting back scattered electrons produced from the pattern by the irradiation of the electron beam by said electron beam irradiating means, wherein said signal arithmetic processing means quantifies a property of the three-dimensional shape of the pattern as a feature index on the basis of a signal of the secondary electrons detected by said secondary electron detecting means, and a signal of the back scattered electrons detected

by said back scattered electron detecting means (Shishido, Fig. 10, par. 0099).

Referring to claim 5, the system according to claim 1, wherein said device property estimating means evaluates the degree of similarity between the feature indices of the three-dimensional shape of the pattern, which have been quantified by said a feature index calculating means, and the feature indices of each three-dimensional pattern shape, which have been recorded in the database (Ponnapalli et al., Fig. 6, col. 7, ll. 16 -34), and estimates device properties of a circuit containing patterns each having a feature index high in the degree of similarity, as the properties of the device circuit formed by the pattern to be evaluated (Ponnapalli et al. , col. 3, ll. 45 to col. 4, ll. 20; Figs. 2-5, col. 5, ll. 12 to col.7, ll. 34).

Referring to claim 6, the system according to claim 1, wherein said device property estimating means estimates the three-dimensional pattern shape, based on the feature indices of the three-dimensional pattern shape, which have been calculated by said feature index calculating means (Ponnapalli et al. , Figs. 2 and 4; col. 5, ll. 12 to col. 6, ll. 31), and estimates the properties of a device circuit formed by the pattern to be evaluated, based on feature indices of a three-dimensional shape at an arbitrary specific point (“a valid pair”), of the estimated three-dimensional pattern shape (Ponnapalli et al. , Figs. 2 and 4; col. 5, ll. 12 to col. 6, ll. 31).

Referring to claim 10, Shishido discloses a method for evaluating a semiconductor device pattern, comprising the following steps of:

irradiating a converged electron beam onto a pattern to be evaluated, while scanning the same (par. [0026]-[0028]; Fig. 10, par. [0097]-[0099]);

detecting secondary electrons produced from said pattern by the irradiation of the electron beam (Fig. 10, par. [0097]-[0099]);

dividing a signal waveform obtained by the detection of the secondary electrons into a plurality of regions, based on an amount of change in signal amount of the signal waveform (Figs. 11 and 25, paragraphs [0099]-[0100]) ;

quantifying properties of a three-dimensional shape of the pattern to be evaluated, as a feature index on the basis of the size of said each divided region (Figs. 8 and 11, paragraphs [0099]-[0104]);

Shishido does not discloses:

estimating properties of a device circuit formed by the evaluated pattern from said quantified feature indices of pattern to be evaluated, on the basis of a relationship between pre-stored feature indices of each three-dimensional pattern shape and device properties of a circuit containing patterns each having the feature index.

Ponnapalli discloses:

estimating properties of a device circuit formed by the evaluated pattern from said quantified feature indices of pattern to be evaluated, on the basis of a relationship between pre-stored feature indices ("wire widths") of each three-dimensional pattern shape and device properties ("capacitance") of a circuit containing patterns each having the feature index (Fig. 2; col. 3, line 23 to col. 4, line 20; col. 5, line 55 to col. 6, line 32).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Shishido with Ponnapalli because the combined teaching which including a database contains a library of pre-computed parasitic values

(electrical properties) for each 3-D pattern of wiring and extracting (estimating) the capacitance and inductance (electrical properties) of patterns based on their corresponding pattern indices and the stored information (Fig. 2;col. 3, line 23 to col. 4, line 20; col. 5, line 55- col. 6, line 32) would provide an accurate and speedy computation of interconnect parasitic values both before and after performing a detailed wiring of an IC chip (col. 3, ll. 6-11) .

Referring to claim 11, the method according to claim 10, wherein in said irradiating step, the electron beam is irradiated onto the evaluated pattern from different plural directions (Shishido et al., Fig. 10, par. 0098).

Referring to claim 12, the method according to claim 10, wherein in a step for, in said detecting step, further detecting back scattered electrons generated from the pattern to be evaluated and dividing the same into the plurality of regions (Shishido et al.; Fig. 11, par. 0100), a waveform division is done based on an amount of change in signal amount of the signal waveform obtained by detecting the secondary electrons, and an amount of change in signal amount of a signal waveform obtained by detecting the back scattered electrons (Shishido et al., Fig. 7, par. 0018), and in said quantifying step, the properties of the three-dimensional pattern shape is quantified as a feature index on the basis of a signal obtained by detecting the secondary electrons, and a signal obtained by detecting the back scattered electrons (Shishido et al., Fig. 10, par. 0097-0099).

Referring to claim 13, the method according to claim 10, wherein in said device-circuit property estimating step, the degree of similarity between the feature indices of

the three-dimensional pattern shape, which have been quantified in said quantifying step (Ponnapalli et al., Fig. 6, col. 7, ll. 16 -34), and the pre-stored feature indices of each three-dimensional pattern shape is evaluated to thereby estimate device properties of a circuit containing a pattern having a feature index high in the degree of similarity as the property of the device circuit formed by the pattern to be evaluated (Ponnapalli et al. , col. 3, ll. 45 to col. 4, ll. 20; Figs. 2-5, col. 5, ll. to col.7, ll. 34).

Referring to claim 14, the method according to claim 10, wherein in said device-circuit property estimating step, the three-dimensional shape of the pattern to be evaluated is estimated based on the feature indices of the three-dimensional pattern shape, which have been quantified in said quantifying step (Ponnapalli et al., Figs. 2 and 4; col. 5, ll. 12 to col. 6, ll. 31), and the properties of a device circuit formed by the pattern to be evaluated is estimated based on feature indices of a three-dimensional pattern shape at an arbitrary specific point ("a valid pair"), of the estimated three-dimensional pattern shape (Ponnapalli et al. , Figs. 2 and 4; col. 5, ll. 12 to col. 6, ll. 31).

8. **Claims 7-8 and 15-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Shishido et al. (" Shishido") (Pub. No. 2003/0015660) in view of Ponnapalli et al. ("Ponnapalli") (US Patent No. 6175947) and in further view of Solomon et al. ("Solomon")(US Pat. No. 5,900,663).

Referring to claim 7 and similarly recited claim 15, Shisido and Ponnapalli substantially disclose the limitations of claim 7 and 15, respectively.

However, Shisido and Ponnapalli do not teach each pattern in a circuit having the feature index in the form of a function by a regression analysis.

Solomon teaches a regression analysis technique can be used to extracting optimal model parameters (col. 8, ll. 64 to col. 9, ll.16) for analyzing patterned samples of semiconductor integrated circuits to determine the thickness and composition of layers fabricated during manufacture (abstract; col. 3, ll. 15-20; col. 8, ll. 64 to col. 9, ll.16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Shishido and Ponnapalli with the teaching of Solomon because utilizing the regression analysis would provide a fast and practical method for analysis of patterned samples of semiconductor circuits (Solomon, abstract)

Referring to claim 8 and similarly recited claim 16, Shisido and Ponnapalli substantially disclose the limitations of claims 8 and 16, respectively.

However, Shisido and Ponnapalli do not teach three-dimensional pattern shape feature index determined by a regression analysis.

Solomon teaches a regression analysis technique can be used to extracting optimal model parameters (col. 8, ll. 64 to col. 9, ll.16) for analyzing patterned samples of semiconductor integrated circuits to determine the thickness and composition of layers fabricated during manufacture (abstract; col. 3, ll. 15-20; col. 8, ll. 64 to col. 9, ll.16).

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the teachings of Shishido and Ponnapalli with the teaching of

Solomon because utilizing the regression analysis would provide a fast and practical method for analysis of patterned samples of semiconductor circuits (Solomon, abstract).

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tuyen To whose telephone number is (571) 272-8319. The examiner can normally be reached on 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on (571) 272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tuyen To
Patent Examiner
AU 2825

VUTHE SIEK
PRIMARY EXAMINER